Amendments to the drawings

The attached sheet of drawings includes changes to Fig. 31. This replacement sheet replaces the original sheet.

Remarks

Claims 3 and 7-11 have been amended and claims 5 and 6 have been cancelled, with the elements of claims 5 and 6 incorporated into claims 3 and 7-11. Claims 1-4 and 7-11 are currently pending.

Objection to the Drawings

In order to overcome this objection, applicant has revised Fig. 31 as attached, a copy of which is enclosed herewith. In addition, a correction is being made to correct a typographical error to change Data Measurer 10 to Data Decider 10 in accordance with the Specification.

Double Patenting Rejection

Claims 1-6 were rejected on the ground of nonstatutory obviousness type double patenting over claims 1-2, 4-5, 7 and 8 of U.S. Patent No. 7,359,425 to Wada in view of U.S. Patent No. 5,533,010 to Tanaka.

A terminal disclaimer has been submitted such that Wada and the present application will be co-terminated. Thus, Applicant respectfully requests withdrawal of the rejection

Rejection of claims 1-11 under 35 USC §103(a)

Claims 1-6 and 7-11 have been rejected as unpatentable over Japanese Patent Application No. 2002-262680 (referred to as AAPA) in view of U.S. Patent No. 5,533,010 to Tanaka.

Independent claims 1, 7, 9 and 11

The Examiner alleges that Fig. 31 of AAPA discloses "a delay time controller for generating a periodic pulse, inputting the periodic pulse to a first matched filter, outputting the periodic pulse to a second matched filter when transmission data has a first level out of 2 logical levels, outputting the periodic pulse to a third matched filter when the transmission data has a second level out of the 2 logical levels" as recited in claims 1, 7, 9 and 11 of the present invention.

However, paragraph [0004] of AAPA discloses "According to this method, as illustrated in FIG 31, in a transmitter, a delay time controller 2 generates a pulse based on a transmission data signal, and outputs output signals Kl to K3 to matched filters 1-1 to 1-3 of

FIG 4, respectively." and Fig. 31 of AAPA shows that a delay time controller 2 outputs an output signal KI to a matched filter 1-1, an output signal K2 to a matched filter 1-2 and an output signal K3 to a matched filter 1-3.

Therefore, Fig. 31 of AAPA simply shows that the delay time controller 2 outputs the output signals K1-K3 to the matched filters 1-1 and 1-3, respectively. However AAPA fails to disclose outputting the periodic pulse to the second matched filter when the transmission data has a first level out of 2 logical levels as recited in claims 1, 7, 9 and 11 of the present invention and outputting the periodic pulse to the third matched filter when the transmission data has a second level out of the 2 logical levels. Namely, nowhere does AAPA disclose conditions for outputting the periodic pulse to the second/third matched filters. Also, Tanaka fails to disclose this feature.

Therefore, a prima facie case of unpatentability is not established. For at least the above reasons, claims 1, 7, 9 and 11 and claims depending therefrom should be deemed allowable.

Independent claims 3, 8, 10 and 11

The Examiner alleges that Fig. 31 of AAPA discloses "wherein the delay time measurer comprises a first circuit for receiving the first output signal and calculating a square value or an absolute value of the first output signal, a second circuit for receiving the second output signal and calculating a square value or an absolute value of the second output signal, a first latch for receiving and setting a output signal of the first circuit, a second latch for receiving and setting a output signal of the second circuit, a first memory for reading a output signal of the second latch as the detection result by receiving a output signal of the first latch, a second memory for reading the output signal of the first latch as the detection result by receiving the output signal of the second latch, and a reset section for outputting a reset signal by receiving outputs of the first and second latches" as recited in amended claims 3, 8, 10 and 11 of the present invention.

However, paragraph [0006] of AAPA discloses "a delay time measurer 9 determines which of the output signals SI and S2 was received first" and Fig. 31 shows that the delay time measurer 9 receives signals SI and S2 and outputs signals QI and Q2.

Therefore, AAPA discloses that the delay time measurer 9 determines which of the output signals SI and S2 was received first, however, fails to disclose how to generate a detection result for use in a data decider using the first output signal and the second output signal. That is AAPA fails to disclose "wherein the delay time measurer comprises a first

circuit for receiving the first output signal and calculating a square value or an absolute value of the first output signal, a second circuit for receiving the second output signal and calculating a square value or an absolute value of the second output signal, a first latch for receiving and setting a output signal of the first circuit, a second latch for receiving and setting a output signal of the second circuit, a first memory for reading a output signal of the second latch as the detection result by receiving a output signal of the first latch, a second memory for reading the output signal of the first latch as the detection result by receiving the output signal of the second latch, and a reset section for outputting a reset signal by receiving outputs of the first and second latches" as recited in amended claims 3, 8, 10 and 11. Also, Tanaka fails to disclose the above feature.

For at least the above reasons, a prima facie case of unpatentability has not been established and Applicant requests withdrawal of the rejection.

Conclusion

Applicants have made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Kevin McNeely, Applicant's Attorney at (202) 429-3781 so that such issues may be resolved as expeditiously as possible.

For these reasons, and in view of the above amendments, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,

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Date

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